A SINGLE CHIP MONOLITHIC INTEGRATED S-BAND FREQUENCY DISCRIMINATOR

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ABSTRACT

This paper describes a highly integrated MMIC frequency discriminator (3.3 mm x 5.5 mm) for S-band. The discriminator consists of two balanced mixers, three wilkinson power dividers (one of them has integrated a 90° phase shifting network) and one amplifier. To ensure a certain frequency resolution, several discriminators with different delay lines have to be connected into a parallel configuration. An into the discriminator integrated amplifier enables distributed amplification and reduces the specifications for the driving limiting amplifier. The high performance achieved and the small die size makes this discriminator suitable for integration into IFM systems.

INTRODUCTION

Frequency discriminators are one building block in every Radar warning receiver. To our knowledge, the in fig. 1 shown MMIC is the first completely monolithically integrated frequency discriminator on one chip, which covers the frequency range from 2 to 4 GHz. Fig. 2 shows the block diagram of a frequency discriminator with a specific frequency resolution. The block diagram of our monolithically realized frequency discriminator is shown in fig. 3.

A comparison of the block diagrams shows, that the frequency discriminator of fig. 2 consists of five identically discriminators of fig. 3 connected with different delay lines (DL1 to DL5) and some additional power dividers (PD).

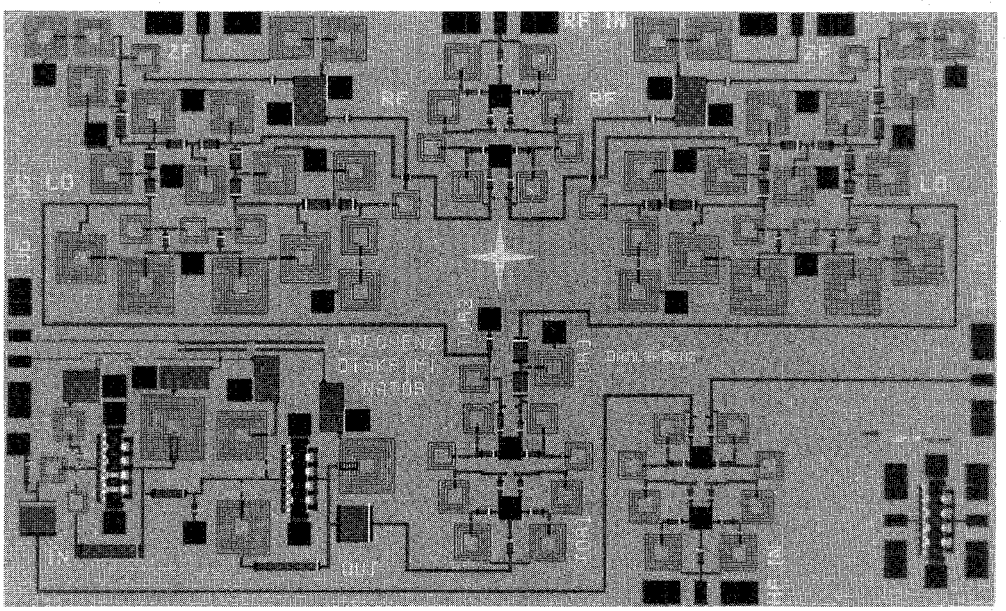

Fig. 1: Photograph of the monolithic frequency discriminator. Chip size is 3.3 mm x 5.5 mm.

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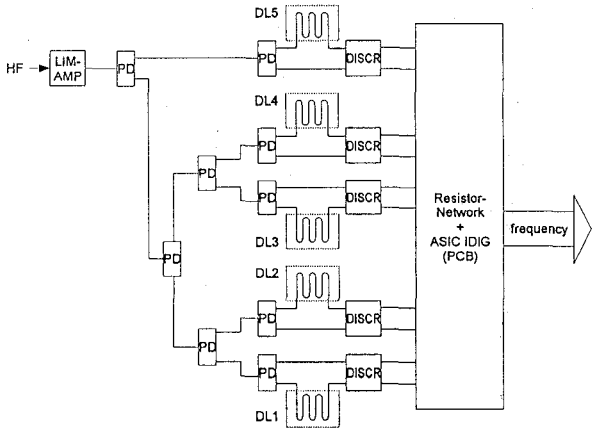

Fig. 2: Block diagram of the frequency discriminator

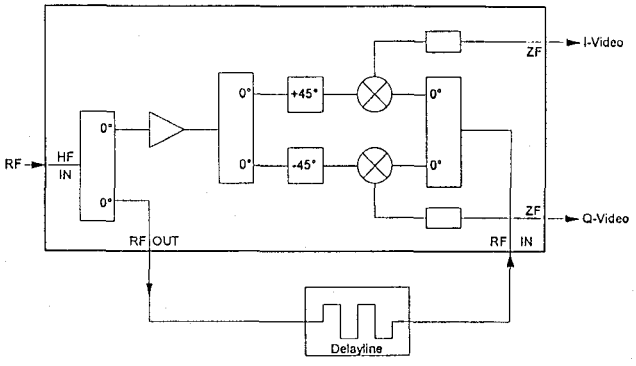

Fig. 3: Block diagram of the monolithic frequency discriminator

PROCESS DESCRIPTION

The MMIC was realized in a mature, 0.5 micron ion implanted MESFET process of the Daimler-Benz foundry that includes via holes, epitaxial thin film resistors and MIM capacitors. The technology allows integration of MESFETs and good mixer diodes on the same chip and has been published else where /1/. Gates are written with E-beam lithography. This technology provides high yields in a 3" wafer process for both active and passive components.

FREQUENCY DISCRIMINATOR CIRCUIT DESCRIPTION

The frequency discriminator, shown in fig. 1, consists of 3 Wilkinson dividers, a 2-stage amplifier and two balanced mixers. The complete circuit contains more than 120 spiral inductors, MIM-capacitors and resistors. The design of the components of the frequency discriminator has been optimized to fulfil system specifications and to minimize chip area.

WILKINSON DIVIDER

The Wilkinson dividers are realized with lumped elements. Distributed structures will become to large for realization on GaAs in the frequency range around 3 GHz. A two stage tandem structure is chosen to get better performance for this broadband (2 to 4 GHz) divider /2/. Symmetrical power dividing and 90° phaseshift is realized with high pass and low pass networks at the output ports. Fig. 4 shows measured typical results; transmission loss is 4 dB at the dividing ports and isolation of the output ports in better than 25 dB.

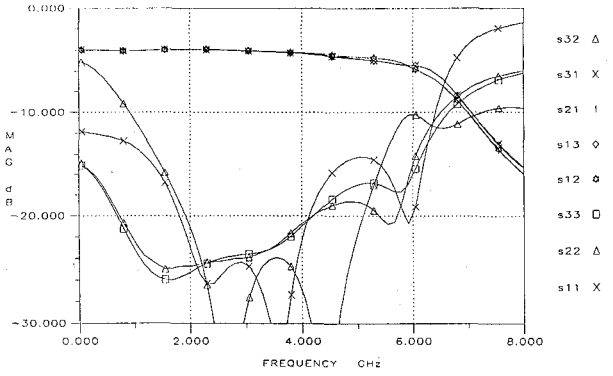

Fig. 4: Measured transmission loss and return loss of the Wilkinson divider versus frequency

AMPLIFIER

A two stage feedback amplifier was chosen to achieve a gain of more than 20 dB. The MESFET gatewidth of each stage is 1000 micron. Fig. 5 shows measured typical results of more than 20 dB gain from 1 to approximately 6 GHz. Input and output return loss is better 10 dB in the desired frequency range. The 1 dB compression point is higher 17 dBm.

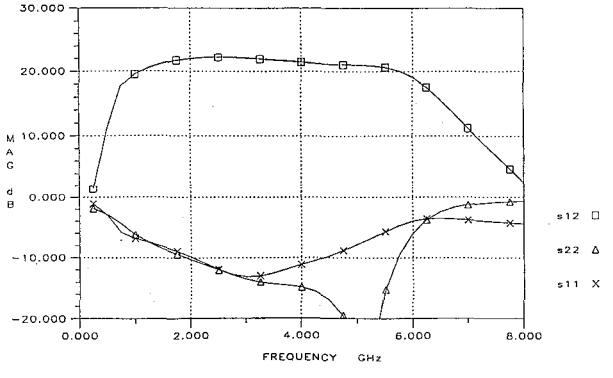

Fig. 5: Measured gain and return loss of the amplifier versus frequency

180° HYBRID

The 180° hybrid is realized as ratrace coupler with lumped elements /3/. The coupling arms of the ratrace are extended to π and T-structures to enhance the bandwidth /4,5/. Fig. 6 shows measured typical results; transmission loss is approximately 4 dB and isolation is better than 19dB.

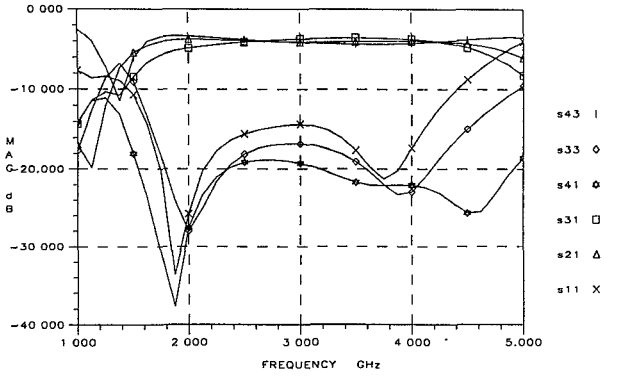

Fig. 6: Measured transmission loss and return loss of the 180° Hybrid versus frequency

BALANCED MIXER

Matching circuit of the mixer diode (6 finger, length of 5 micron each) and the low pass filter in the IF-output are realized with lumped elements. The large signal input impedance of the mixer diode is calculated by using an inhouse model. The comparison of the calculations and measurements of the conversion loss of a single ended mixer shows excellent agreement. The balanced mixer has a measured conversion loss of less than 5 dB at 3 GHz as shown in figure 7. Power consumption for the LO is approximately

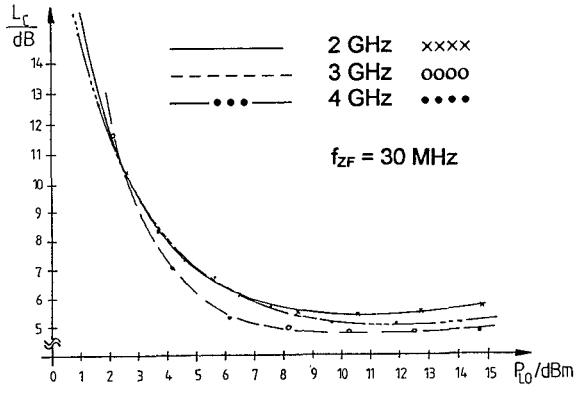

Fig. 7: Measured conversion loss of the balanced mixer versus LO

10 dBm. Fig. 8 shows the measured conversion loss versus LO/RF frequency at IF frequency of 30 MHz and LO power of 10 dBm.

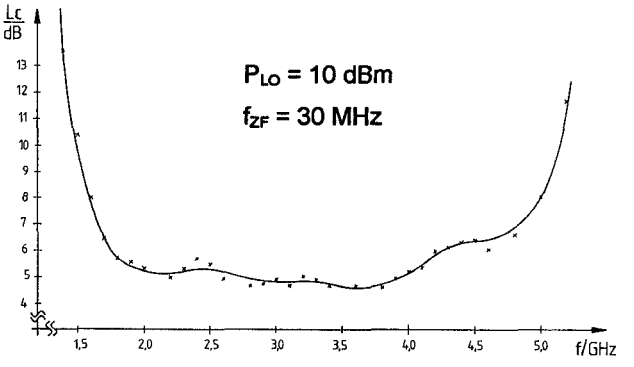

Fig. 8: Measured conversion loss of the balanced mixer versus LO/RF frequency

FREQUENCY DISCRIMINATOR

The RF signal at port HF IN is splitted in a first Wilkinson divider into the LO and RF path. The LO part of the RF signal is amplified and after a second splitting and 90° phaseshifting fed to the LO ports of the two balanced mixers. The other part of the RF signal is phaseshifted versus an external line between port RF OUT and RF IN. The RF signal is then splitted by a third divider and fed to the RF ports of the balanced mixers.

MEASURED DISCRIMINATOR RESULTS

Measurements are performed on wafer with an external coaxial line having a length of approximately 1 m (3ft 3"). An external amplifier was inserted between the coaxial line and the port RF IN to compensate line loss and to get a stronger IF signal. Measured results for the two IF signals (channel I and Q) are shown in fig. 9. The desired 90° phaseshift of the two signals resulting in concentric circles of the channel I versus Q plot shown in figure 10 can clearly be seen. Measurements are done with 0 dBm input power at port HF IN and frequency is swept from 2 to 4 GHz. Fig. 9 and 10 show a measured amplitude of more than 700 mV at 50 Ω.

Fig. 11 shows the phase error, that means the deviation from the linear phase versus frequency. As can be seen the maximum error from 2 to 4 GHz is less than ± 12° at room temperature. From 0 to 100°C the phase error is below ± 16.5° without any temperature compensation.

The frequency resolution of the discriminator depends on the number of stages and the length of the delay

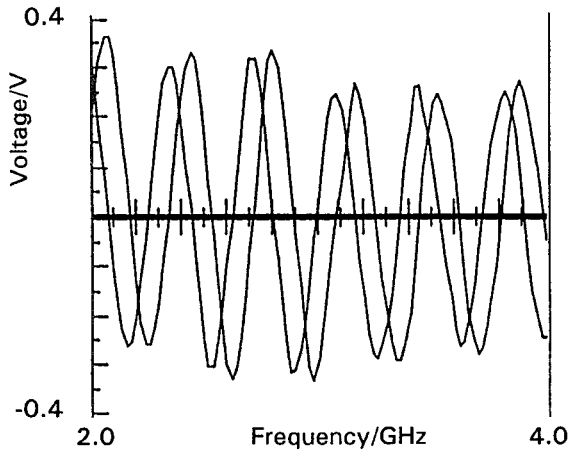

Fig. 9: Measured IF signals in mV at the I and Q channel versus frequency

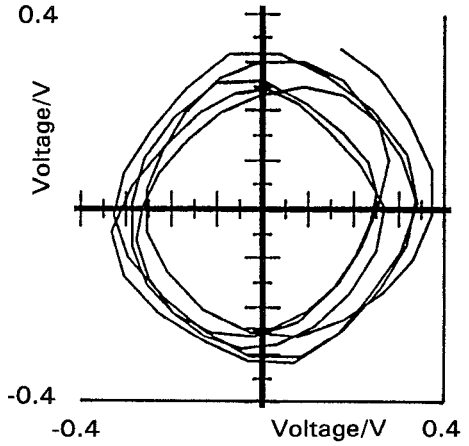

Fig. 10: Polar display of the IF signals

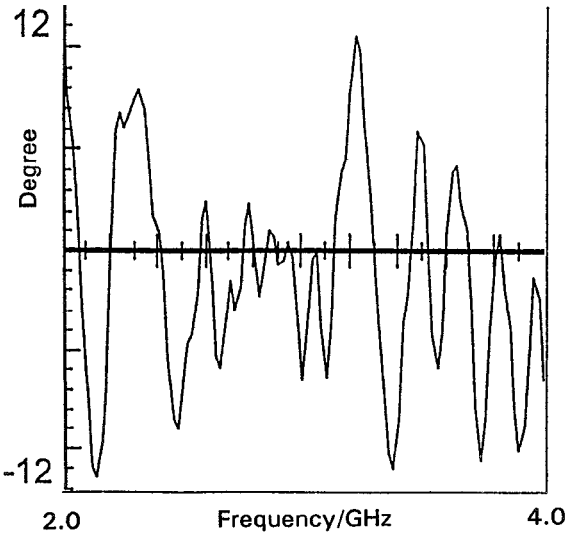

Fig. 11: Phase error versus frequency

lines as shown in the blockdiagram of fig. 2. The frequency accuracy depends strongly on the measured phase error shown in fig. 11. The hybrid realized discriminator with a comparable phase error has a measured frequency accuray of some MHz.

The yield of the passive circuits like Wilkinson divider or hybrid coupler is above 75%. The two stage amplifier reaches more than 50% and the yield for the large frequency discriminator chip is around 20%.

CONCLUSION

We have demonstrated a monolithically integrated frequency discriminator on one chip. The chip area is approximately 18 mm^2. The high performance achieved allows its integration into IFM systems. This design demonstrates the ability offered by the MMIC technology to achieve high performance circuits with a high level of integration and low DC power consumption.

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